ECE 150 Digital Logic Design, Fall 2022

Final Exam, November 30th 2022 Name: _____

The exam has 100 pts. Closed book, no calculators. Write all answers and show all work inside your blue book for partial/full credit. ***Read carefully.***

Problem 1 (10 pts).
Implement the XOR circuit using only NAND gates.

Problem 2 (5 pts).
Give the truth-table of a tri-state buffer and briefly describe its behavior. Under what circumstances are they useful?

Problem 3 (10 pts).
Consider the circuit shown in Figure 1, with a D-latch and Master-minion D Flip-Flop. Complete the timing for outputs Q_L and Q_F.

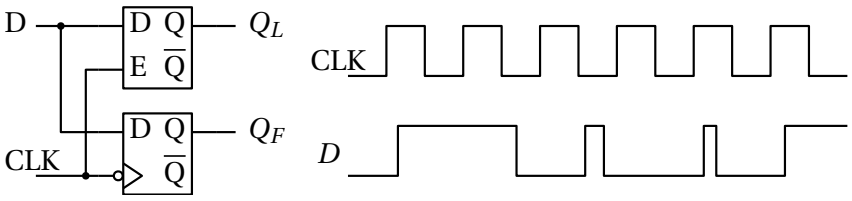

Figure 1: D-latch and MM D-FF circuit with corresponding input timing diagram.

Problem 4 (15 pts).
Consider the circuit shown in Figure 2 below, consisting of a 4 bit full adder with external XOR gates. The circuit has been implemented and supplied with test inputs, and the observed logic value of each wire has been labeled on the diagram.

(a) Are the circuit components functioning correctly? Why or why not? What is the correct output of the circuit?

(b) Convert the binary inputs and outputs to decimal. What arithmetic operation does the (corrected) circuit perform?

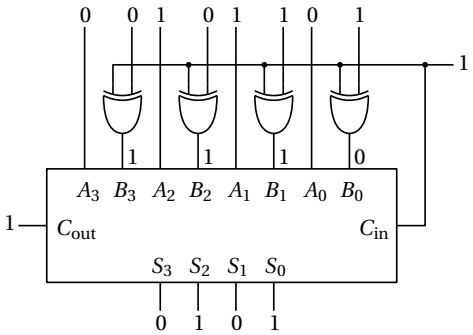

Figure 2: 4 bit full adder with external gates. Observed logic values labeled on each node.

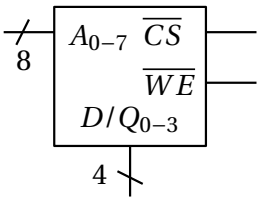

Figure 3: 4x256 RAM chip.

Problem 5 (20 pts).
Using several of the 4x256 RAM chip shown in Figure 3 and any additional combinatorial circuitry (muxes, gates, etc.), implement an equivalent 8x1024 RAM chip. Carefully label your equivalent circuit's write-enable (not), chip-select (not), input/output, and address pins. Indicate MSB and LSB on your address pins.

Problem 6 (15pts).
Consider the Mod-N counter in Fig. 4 below. The RC circuit connected to $\overline{R}$ forces the flip-flops (FFs) to be reset on start-up, hence we know our circuit starts in the 000 state.

(a) Is this circuit synchronous or asynchronous?

(b) With FF outputs labeled $Q_2Q_1Q_0$ left to right, draw a timing diagram to determine the states of the counter.

(c) Denote the FF states below your timing diagram in decimal, interpreting Q_2 as the MSB and Q_0 as the LSB.

(d) What Mod is the counter?

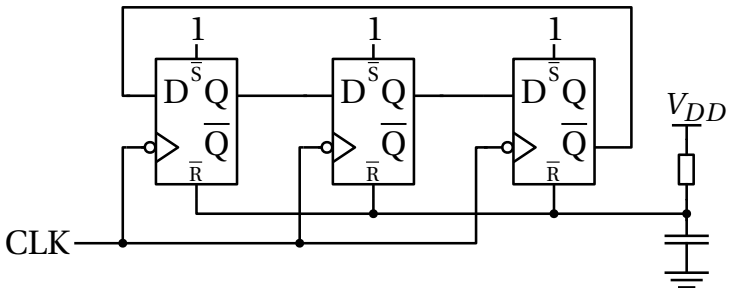

Figure 4: Counter circuit with start-up reset configuration.

Problem 7 (20 pts).
In this problem, you will build a "resetable" synchronous Mod-4 binary up counter with JK flip-flops, which *transitions to zero* when an input signal R is high, and otherwise continues counting up (with wrap-around).

(a) Construct a state transition diagram for your counter.

(b) Convert your state transition digram to a table, labeling current states, inputs, control variables, and next states. Determine values for your control variables to achieve the desired transitions.

(c) Determine simplified boolean expressions for your control variables.

(d) Draw a logic diagram of your circuit. Label the clock, R, and your state variables clearly.

Problem 8 (5 pts).
Consider the "resetable" Mod-4 synchronous circuit constructed in the previous problem. Using this counter, design a *programmable* synchronous counter, in which a supplied number $P = P_1P_0$ determines the maximum value of the counter. What is the mod of the counter in terms of P?