ECE 150 Digital Logic Design, Fall 2022

Midterm Exam, October 19th 2022 Name: _____

The exam has 100 pts. Closed book, no calculators. Write all answers and show all work inside your blue book. Read carefully.

Problem 1 (5 pts).
Convert the following to the specified number system.

(a) FAB_{16} to Octal.

(b) $1010\ 1101_2$ to Decimal.

(c) 808_{10} to Binary.

(d) 65_{10} to Hexadecimal.

(e) 210_3 to Decimal.

Problem 2 (5 pts).
Perform the following computation, $18_{10} - 32_{10}$, in a two's compliment binary number system. Verify that your answer is correct by converting your answer back to decimal.

Problem 3 (14 pts).
Consider the following boolean expression,

$$X = \overline{\overline{A} + B} + A(\overline{\overline{B} + BC}) + (A + \overline{C})\overline{A}B\overline{C}D$$

(a) Write X in sum-of-products form.

(b) Convert X to a truth-table.

(c) Use a Karnaugh-map to simplify X from its truth table.

(d) Draw a logic diagram for the simplified expression. Label all inputs and outputs.

Problem 4 (8 pts).

(a) Write the truth-table and corresponding boolean expression for a 2:1 multiplexer.

(b) Draw the logic diagram of a 4:1 mux using 2:1 muxes.

(c) Draw the logic diagram of a 16:1 mux using 4:1 muxes.

Problem 5 (20 pts).
In this problem, you will build a digital comparator that takes two N-bit binary numbers, A and B, and sets separate pins E, G, or L to high if $A = B$, $A > B$, or $A < B$, respectively.

(a) Write the truth-table for a *half-comparator* which takes as input two 1-bit binary numbers, A and B, and outputs E, G, and L.

(b) Determine boolean expressions of E and G. Express L in terms of E and G.

(c) A 1-bit *full-comparator* optionally takes as input the E and G results from another comparator (acting on more significant bits). Determine boolean expressions for the E, G, and L outputs of a 1-bit full-comparator in terms of A, B, E_{in}, and G_{in}.

(d) Draw a logic diagram for the 1-bit full-comparator. Draw a corresponding symbol to represent it.

(e) Draw a logic diagram for a 4-bit full-comparator, comparing $A_3A_2A_1A_0$ to $B_3B_2B_1B_0$ (left MSB), using 1-bit full comparators. Label all inputs and outputs. Do not leave input pins floating.

Problem 6 (4 pts).
Describe similarities and differences between the *Gated D-latch* and the *Master-Minion D Flip-Flop*.

Problem 7 (24 pts).
In this problem, you will build a Mod-4 binary up/down counter with positive edge-triggered D flip-flops. The direction of counting is to be controlled by a selection input S, where $S = 0$ denotes up counting and $S = 1$ denotes down counting. Counting must loop around if inputs are not changed.

(a) Construct a state transition diagram for your counter.

(b) Convert your state transition digram to a table, labeling current states, inputs, control variables, and next states. Determine values for your control variables to achieve the desired transitions.

(c) Determine simplified boolean expressions for your control variables.

(d) Draw a logic diagram of your circuit. Label the clock, S, and your state variables clearly.

Problem 8 (20 pts).
Consider the circuit in Figure 1, consisting of a Mod-4 binary up/down counter and a JK flip-flop, where the counter operates as specified in the previous problem. Suppose that the circuit is initialized with the counter in the $Q_1Q_0 = 2_{10}$ state and the JK FF in the 0 state.

(a) Is this circuit synchronous or asynchronous? Why or why not?

(b) Draw a timing diagram of Q_1, Q_0, Y, and S with 8 positive edges from the CLK, starting from the above mentioned initialization.

(c) Describe the behavior of the circuit.

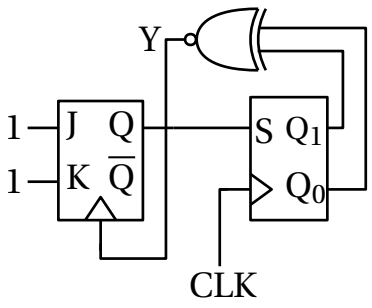

Figure 1: Binary up/down counter with external JK flip-flop.