ECE 150 Digital Logic Design, Fall 2022
Quiz 2, October 12th 2022

Problem 1 (10 pts)**.**
Consider the Mod-N counter in Fig. 1 below. The RC circuit connected to $\overline{R}$ forces the flip-flops (FFs) to be reset on start-up, hence we know our circuit starts in the 000 state.

(a) (2 pts) Is this circuit synchronous or asynchronous?
(b) (6 pts) With FF outputs labeled $Q_2Q_1Q_0$ left to right, draw a timing diagram to determine the states of the counter.
(c) (1 pts) Denote the FF states below your timing diagram in decimal, interpreting Q_2 as the MSB and Q_0 as the LSB.
(d) (1 pts) What Mod is the counter?

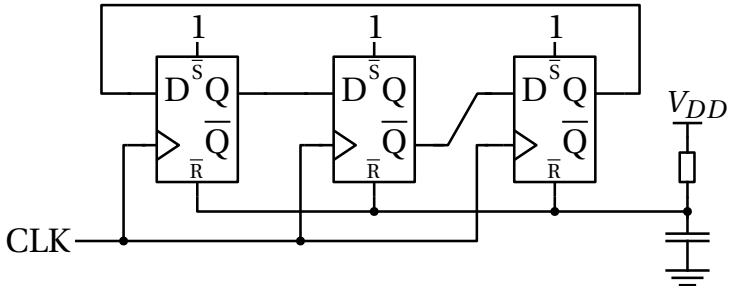
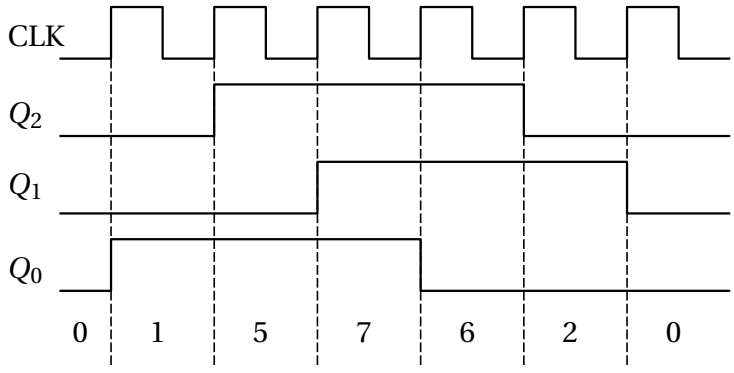


Figure 1: Counter circuit with start-up reset configuration.

Solution.

(a) Synchronous. All elements are driven by the same clock.
(b) Positive edge-triggered (1 pt). Start at 0 (1 pt). Correct answer (4pt).



(c) (see diagram)
(d) Mod-6 as there are unique 6 states.

Problem 2 (10 pts)**.**
Consider the circuit in Fig. 2, where inputs S and D are also driven by the clock-signal.

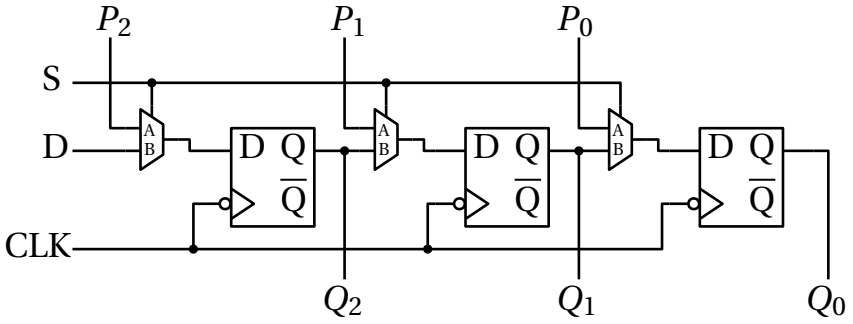
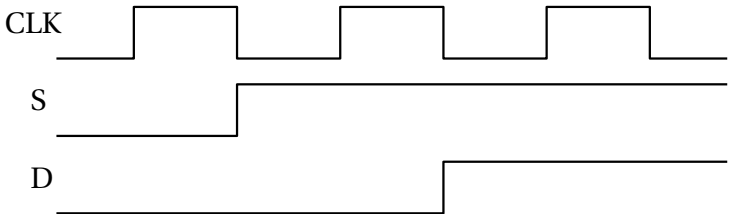


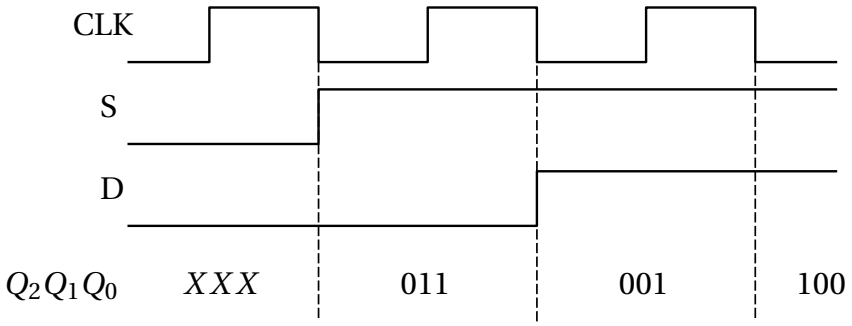
Figure 2: 3-bit register with multiplexers.

(a) (2 pts) Is this circuit synchronous or asynchronous?
(b) (8 pts) Given $P_2P_1P_0 = 3_{10}$, complete the timing diagram below to determine the state of the FFs $Q_2Q_1Q_0$ at each clock-cycle. Assume the 2:1 muxes select input A when $S = 0$.



Solution.

(a) Synchronous. All elements are driven by the same clock.
(b) The multiplexer selects between parallel and serial load. S starts low, so we will load in $Q = P = 011$ at the first negative edge. At the second negative edge, $S = 1$ and $D = 0$, hence will shift in a zero ($Q = 001$). At the third negative edge, $S = 1$ and $D = 1$, so we shift in a 1, ($Q = 100$).



- (1 pt) negative edge triggering.
- (1 pt) don't care / unknowns before first trigger.
- (2 pt) parallel loading of P first.
- (4 pt) correct answer