ECE 150 Digital Logic Design, Fall 2022
Quiz 4, November 23rd 2022

Problem 1 (20 pts)**.**
A bidirectional shift-register (BSR), a.k.a a universal shift-register, is one in which bits can be shifted left or right depending on an input signal S.

(a) With $S = 0$ as right-shifting, and $S = 1$ as left-shifting, design a 4-bit SISO BSR using master-minion D flip-flops. You may use combinatorial circuits that we have learned in class to aid your design. Carefully label your left bit input/output D_L/Q_L, right bit input/output D_R/Q_R, direction selection S, and clock input C_p.

(b) Consider a "Pong" paddle circuit, in which we represent a ping-pong paddle as a set of M contiguous high-bits in an N bit BSR. As we never want to "lose" our ping-pong paddle, we want to use a BSR with the additional constraint that paddle-bits cannot exit the BSR. Augment a BSR circuit to satisfy this constraint, assuming a paddle of 1s is already loaded into the register. Present your final answer in terms of a logic diagram around an encapsulated BSR circuit, labeling all inputs and outputs.

Problem 2 (25 pts)**.**
Suppose you have a single 1-bit full adder circuit (inputs: A, B, C_{in}, outputs: S, C_{out}) and as many MM D flip-flops at your disposal as you'd like (in single FF form and/or register form).

(a) Construct a sequential circuit that performs 4-bit addition between numbers a $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ and stores the resulting value. Label your diagram inputs/outputs, as well as MSB and LSB bit locations. Briefly describe how your circuit is used in terms of loading in your numbers, clocking, and obtaining your answer.

Hint: think about processing one bit at a time.

(b) Augment your 4-bit serial adder circuit to perform 4-bit multiplication, instead of addition. Briefly describe how your circuit is used in terms of loading in your numbers, clocking, and obtaining your answer. How many bits do you need to store your output?