

The exam has 100 pts. Closed book, no calculators. Write all answers and show all work inside your blue book. Show your work for partial/full credit. **Read carefully.**

Problem 1 (5 pts).

Give the truth-table of a tri-state buffer and briefly describe its behavior. Under what circumstances are they useful?

Problem 2 (10 pts).

In the following questions, provide truth tables in terms of current state Q_n , control variables (D or J and K), and next state Q_{n+1} .

- (a) Give the truth table of a positive edge-triggered D flip-flop.
- (b) Give the truth table of a positive edge-triggered JK flip-flop.
- (c) Using a single positive edge-triggered D flip-flop (plus any gates and muxes/demuxes), implement a positive edge-triggered JK flip-flop.
- (d) Using additional gates, how can you augment the circuit from (c) to be negative edge triggered?

Problem 3 (15 pts).

Consider the circuit diagram in Figure 1, with input A , output Y , and state Q_1Q_0 .

- (a) Is the circuit synchronous or asynchronous? Why?
- (b) Determine a boolean expression for Y in terms of the input and state variables.
- (c) Construct a state transition table for the circuit
- (d) Give a corresponding state transition diagram. Ensure each transition arrow is labeled, and that every state bubble contains the value of the state variables.

Problem 4 (15 pts).

Using several of the 1024x8 RAM chip shown in Figure 2 and any additional combinatorial circuitry (muxes, gates, etc.), implement an equivalent 2048x32 RAM chip. Carefully label your equivalent circuit's write-enable (not), chip-select (not), input/output, and address pins. Indicate MSB and LSB on your address pins.

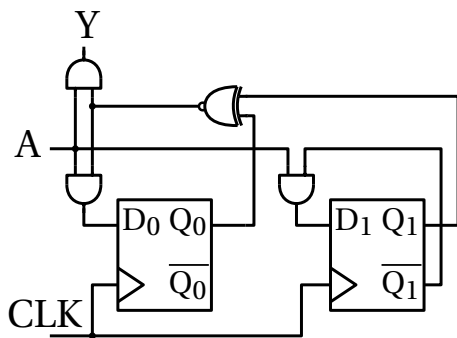


Figure 1: Circuit diagram.

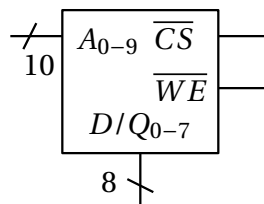


Figure 2: RAM chip.

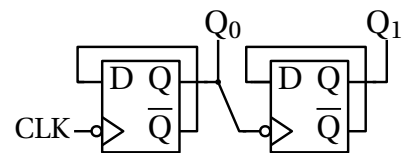


Figure 3: Counter circuit.

Problem 5 (15pts).

Consider the Mod-N counter in Fig. 3. Assume the circuit starts in the $Q_1Q_0 = 00$ state.

- Is this circuit synchronous or asynchronous? Why?
- Draw a timing diagram to determine the states of the counter. Include glitch-states from propagation delay (if they exist).
- Denote the FF states below your timing diagram in decimal, interpreting Q_1 as the MSB and Q_0 as the LSB.
- What Mod is the counter?

Problem 6 (15pts).

A bidirectional shift-register (BSR) is one in which bits are shifted from left to right ($R = 1$) or right to left ($R = 0$) on the edge of a clock pulse, depending on input R .

- Design a 4-bit BSR with edge-triggered D flip-flops. Your BSR should have a left Data-input D_L , right Data-input D_R , a direction pin R , and parallel output pins $Q_0Q_1Q_2Q_3$. You may use gates and muxes/demuxes in your design.
- Briefly describe how you can augment your design to allow for parallel *loading* of data into the register.

Problem 7 (20 pts).

In this problem, you will build a “pause-able” synchronous Mod-4 binary up counter with JK flip-flops, which *pauses counting* when an input signal \overline{P} is low, and otherwise continues counting up (with wrap-around).

- Construct a state transition diagram for your counter.
- Convert your state transition diagram to a table, labeling current states, inputs, control variables, and next states. Determine values for your control variables to achieve the desired transitions.
- Determine simplified boolean expressions for your control variables.
- Draw a logic diagram of your circuit. Label the clock, \overline{P} , and your state variables clearly.

Problem 8 (5 pts).

Consider the “pause-able” Mod-4 synchronous circuit constructed in the previous problem.

- Using pauseable counter(s), implement a Mod-16 synchronous up-counter. Label your most-significant and least significant counters.
- Implement a “chain-able” Mod-4 up-counter, such that the chain-in (C_{in}) pin of a more significant chainable counter could be connected to the chain-out pin (C_{out}) of a less significant chainable counter.