ECE 150 Digital Logic Design, Fall 2023
Homework 2: due October 25th before class

In teams of 2, work through the following problems in JLab. Show your work through equations, diagrams, and sketches of your observations. Hand in a single set of solutions, along with photos of your circuits, on the due date to recieve full credit.

Use the TTL ICs in the lab for the JK flip-flop and Schmitt-trigger!

Problem 1 (555 timer 1)**.**
Given a 555-timer wired for astable operation with components $R_A = 4.7$ kΩ, $R_B = 10$ kΩ, and $C = 680$ pF, determine its frequency and duty-cycle.

Problem 2 (555 timer 2)**.**

(a) Design an astable 555-timer circuit with frequency between $1-2$ Hz and duty-cycle between $1/2 - 2/3$ with resistors and capacitors.

(b) Implement your design using components from the lab. Ensure that the frequency and duty-cycle requirements are still satisfied in your implementation. Display your clock output via an active-low LED.

(c) What effect does changing (i) R_A, (ii) R_B, (iii) C on frequency and duty-cycle? Verify each case in your implementation by swapping component values.

Problem 3 (Button debouncing)**.**

(a) Wire-up a negative edge-triggered JK flip-flop in toggle mode with an active-low LED displaying its output, and a push-button with 1 kΩ pull-up resistor as input to its clock. Sketch an accompanying schematic of this circuit.

(b) Press the button 20 times, recording the JK flip-flop output at the end of each button press. Is the result as expected? Why or why not?

(c) Mechanical buttons exhibit "bouncing" events at their positive and negative edges due to metal to metal contact. If used as input to our circuits, bouncing can trigger an unpredictable number of input events on a single press.

Use an oscilloscope to view the output of your (pull-up) push-button and observe the bouncing phenomenon. Show an example of your button push as observed on the oscilloscope at both positive and negative signal edges.

(d) Resistor-capacitor (RC) circuits can be used to smooth out fast-changing voltages into more slowly varying ones by using the capacitor as a "charge reservoir".

Connect a 10 μF capacitor in parallel to your push-button. How does the observed wave-form change at the output signals positive and negative edges? Would this help with clocking a negative edge-triggered flip-flop? Sketch this new circuit, along with arrows indicating capacitor charge and discharge paths.

(e) The negative push-button signal-edge can be smoothed-out by adding another 1 kΩ resistor, this time to the discharge path of the capacitor (separating the pull-up resistor and the capacitor). Sketch this new circuit (with charge/discharge paths). Wire-up this configuration and verify the behavior (sketch the oscilloscope output). Is signal bouncing and noise completely removed?

(f) Noise present in the RC circuit debouncing may still yield unwanted triggering events in our circuits. Additionally, the capacitor charging and discharging extends the amount of time our voltage levels are neither high enough to be considered logic-high, or low enough to be logic-low (i.e. floating).

A Schmitt-trigger device is one that implements a *voltage-hysteresis* or dual-threshold. One threshold is used for signals transitioning from low to high voltages, and another (lower threshold) is used for signals going from high to low voltages. This difference in thresholds (the **hysteresis-voltage**) allows for noise suppression and removes floating voltage levels by converting all analog voltages into valid digital voltages.

Connect an inverting Schmitt-trigger to the output of your RC debouncing circuit. Sketch your new schematic and show an example of the input and output waveforms of the Schmitt-trigger upon a button press (using two oscilloscope probes). Comment on your observations.

(g) Repeat part (b) with your Schmitt-trigger debounced button clocking the toggle-mode JK flip-flop. We call this configuration a (debounced) **toggle-button**.

You've also seen dual-thresholds (voltage-hysteresis) when we looked inside the 555 timer circuit. For similar reasons, a 555 timer wired in *monostable* mode can also be used for button debouncing, instead of a Schmitt-trigger IC.

Problem 4 (Mod-4 synchronous binary up/down counter)**.**
In this problem, you will design a synchronous counter that changes behavior (up/down counting) based on a button press.

(a) Draw the state-diagram of a Mod-4 binary up/down counter which counts up if external signal $X = 1$, and down if $X = 0$.

(b) Write the state-transition table with D-type flip-flops as your control variables, i.e. D_1D_0 as control variables, Q_1Q_0 as state-variables.

(c) Determine boolean-algebra expressions for D_1 and D_0 in terms of Q_1Q_0 of the current state via boolean algebra simplification and/or Karnaugh-mapping.

(d) Implement and verify your design in logisim.

(e) Wire-up your design with a dual edge-triggered D-type flip-flop IC chip. Verify your design by clocking your circuit manually via an RC-debounced push-button and a logic-probe to check your outputs.

(f) In general, LEDs draw a significant amount of current which may affect the voltages read by other devices. For this reason we do not connect LEDs directly to signals that will be used in other parts of our circuit. Connect outputs Q_1Q_0 to inverters driving active-low LEDs for displaying the current state.

(g) Connect your 555 timer circuit from problem (2) as your counter's clock and your debounced toggle-button from problem (3) as your our direction input X.

Problem 5 (50% duty-cycle)**.**

(a) For the astable 555-timer configuration, what effect does setting $R_B = 0\ \Omega$ have? $R_A = 0\ \Omega$? Is a 50% duty cycle possible with this circuit? Why?

(b) Propose a new 555-timer circuit that has a 50% duty-cycle by using diodes to create symmetric charging and discharging paths. Draw your schematic labeling charge and discharge paths.

(c) Implement your proposed modifications on your circuit from Problem 2.