

Ex

State #	t_n				t_{n+1}	
	Input Var	State var	Output var	Control Var	State var	State #
S	$B_1 B_0$	$Q_2 Q_1 Q_0$	$Y_2 Y_1 Y_0$	$D_2 D_1 D_0$	$Q_2 Q_1 Q_0$	S
S_0	0 X	0 0 0	0 0 0	0 0 1	0 0 1	S_1

Synchronous Sequential Circuit

Moore Machine: $Y = Y(Q)$

Example: $Y = Q$

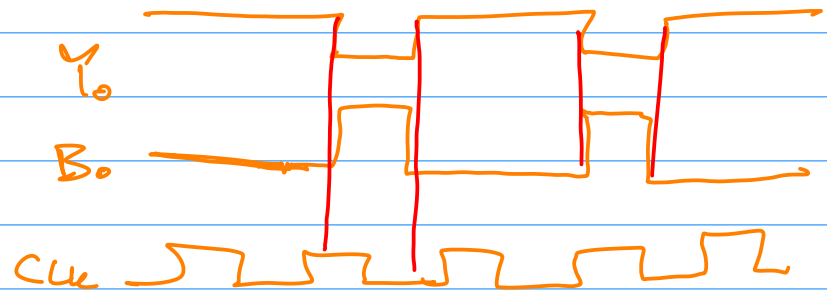
Mealy Machine: $Y = Y(Q, B)$

Combinatorial Circuit $Y = Y(B)$

← Not an FSM

Make Async!

$Q = 000$ $Y_0 = Q_2 Q_1 Q_0 + B_0$



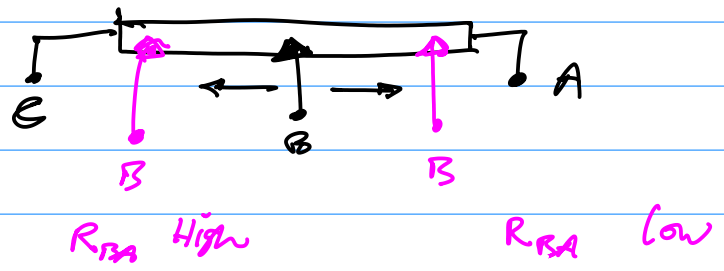
Plan: 1) FSM Block Diagram 2) ADC Extended Example.

Potentiometer

R_A, R_B

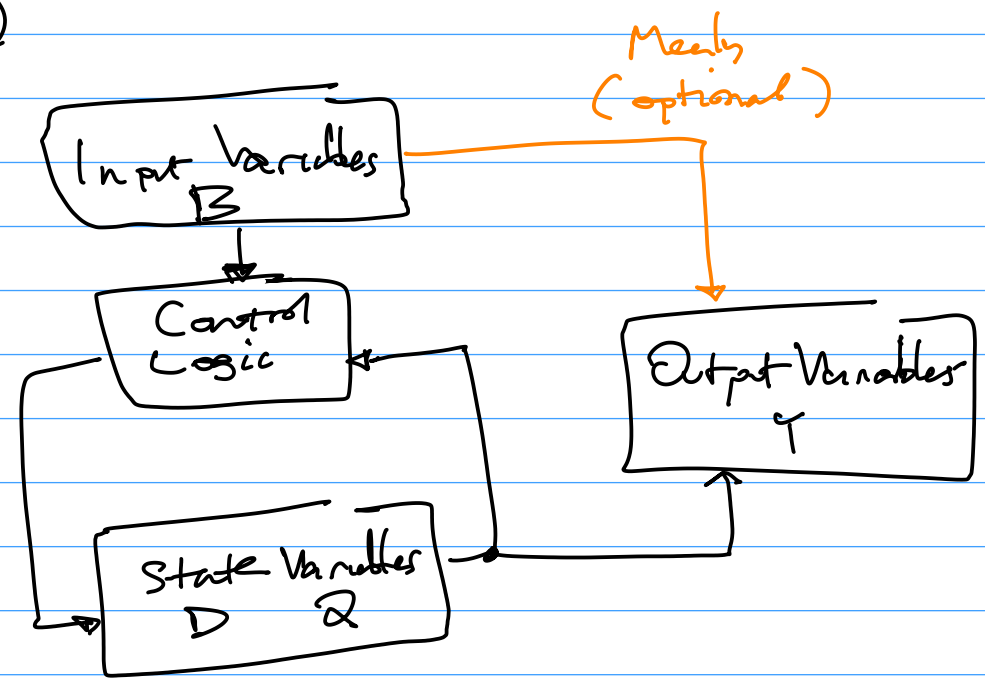
$D = \frac{R_B}{R_A + 2R_B}$

$f = \frac{1}{\log_2 C (R_A + 2R_B)}$

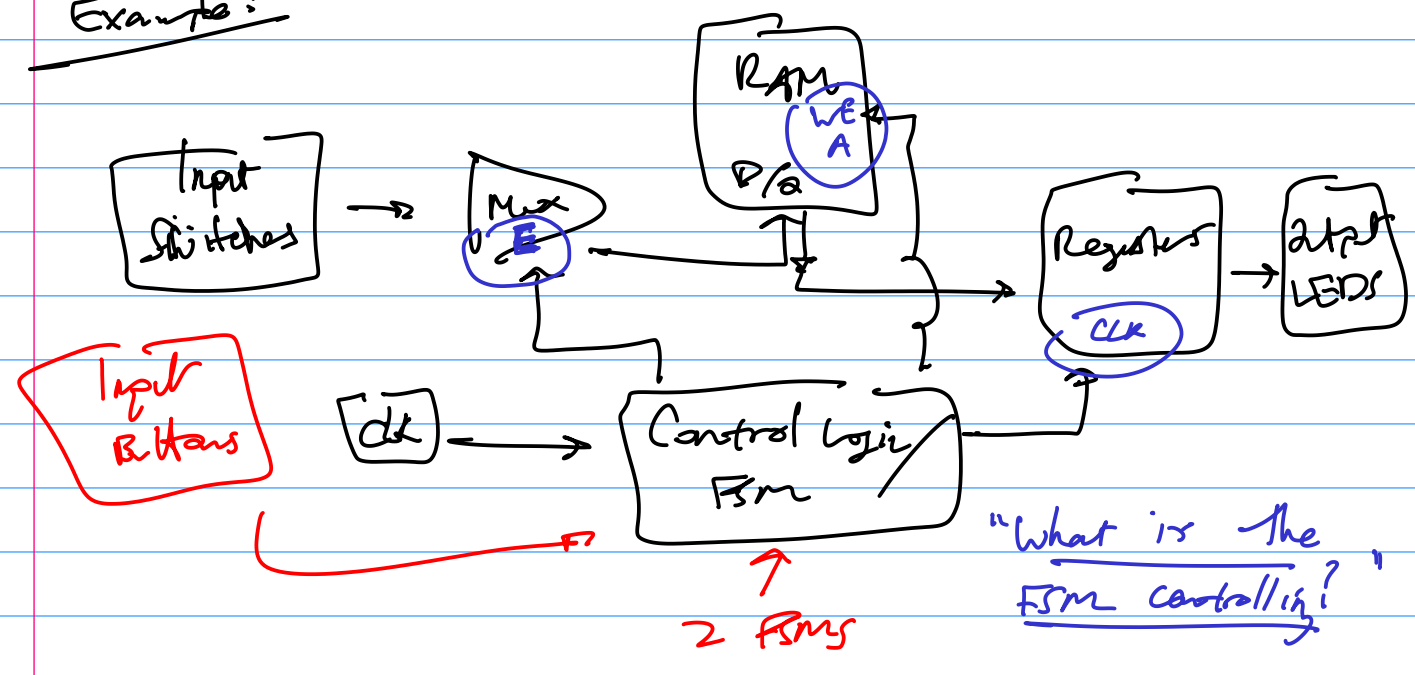


Functional Block Diagram of FSMs

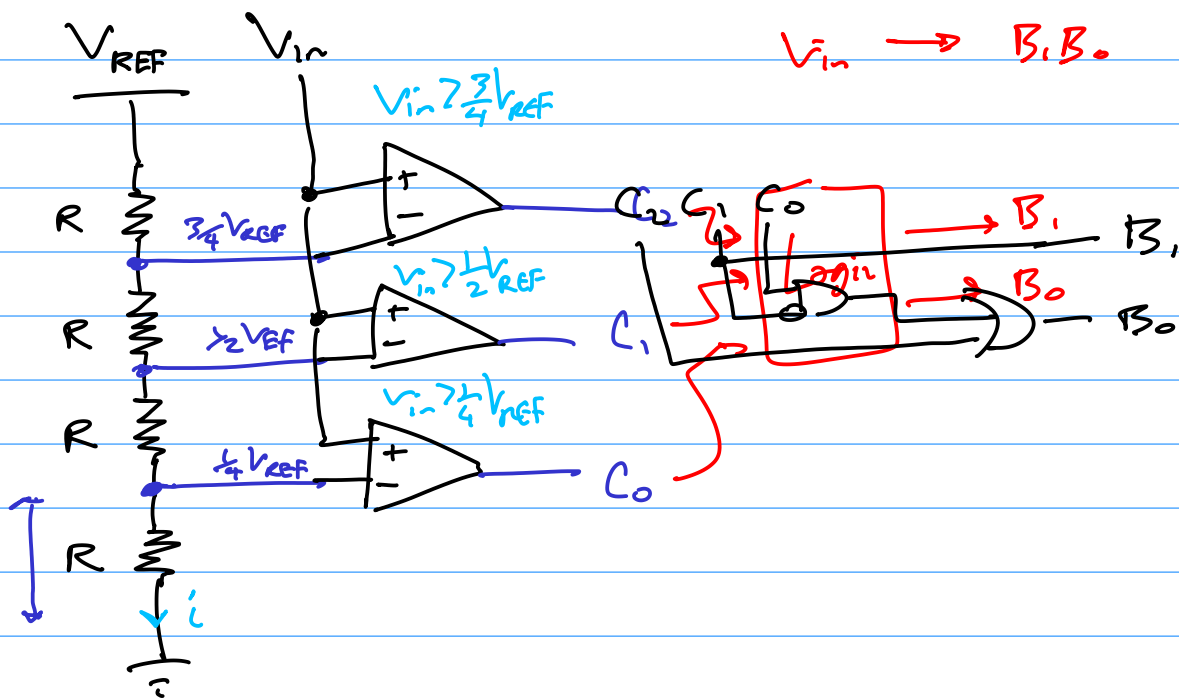
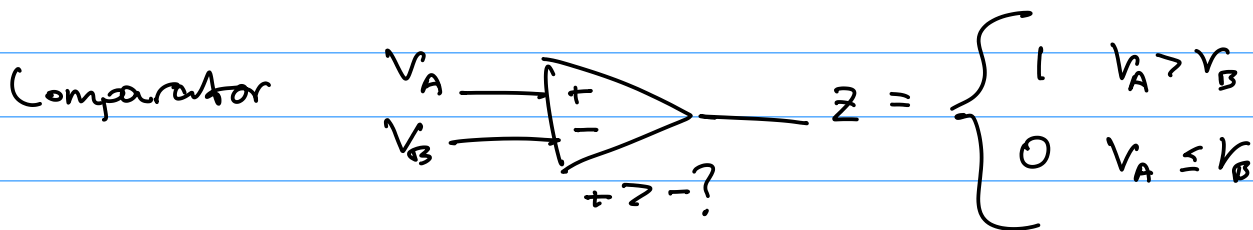
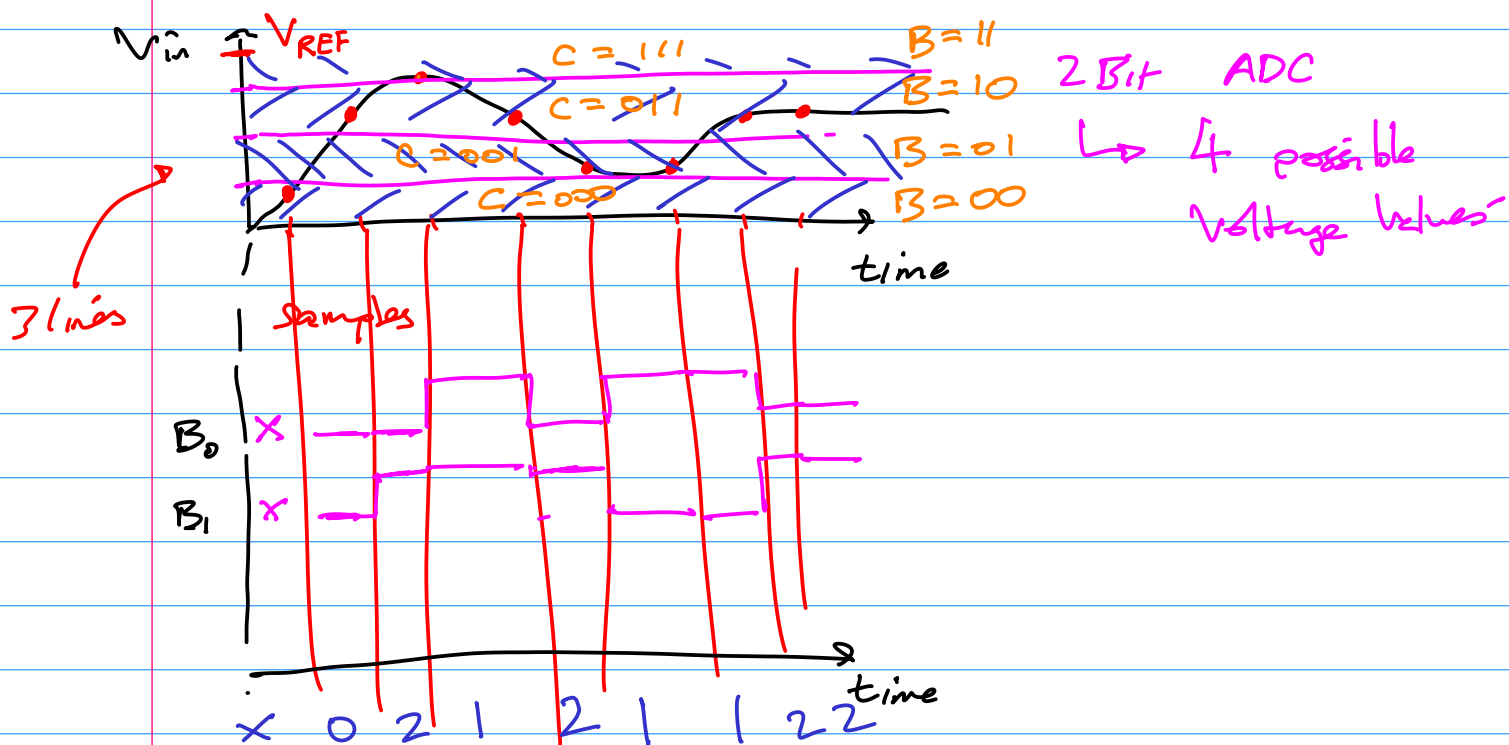
(FBD)



Example:



Analogy to Digital Conversion



$$V = iR = \frac{1}{4} V_{REF}$$

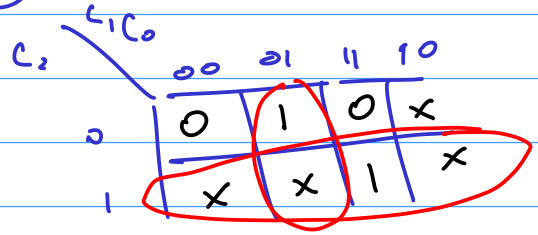
$$V_{REF} = i(R+R+R+R)$$

$$i = \frac{V_{REF}}{4R}$$

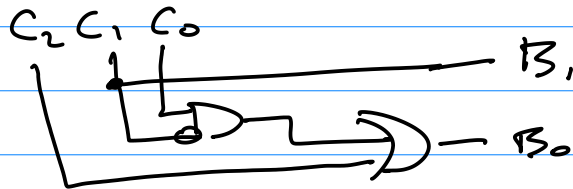
$C_2 C_1 C_0$	$B_1 B_0$
0 0 0	0 0
0 0 1	0 1
0 1 0	X X
0 1 1	1 0
1 0 0	X X
1 0 1	X X
1 1 0	X X
1 1 1	1 1

$$B_1 = C_1$$

B_0



$$B_0 = C_2 + \bar{C}_1 C_0$$

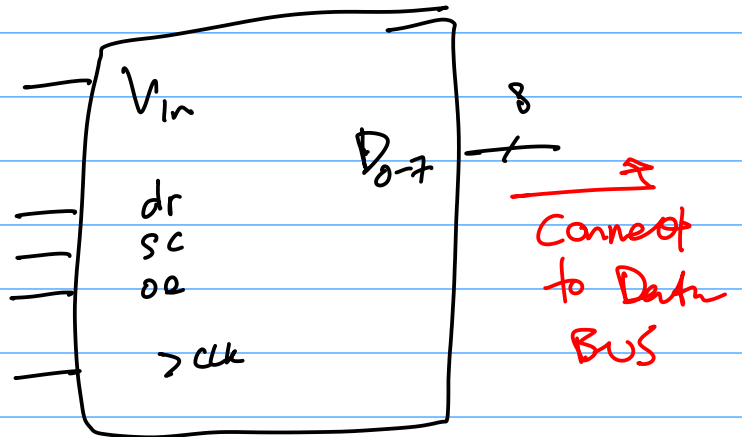


ADC FSM

ADC Chip

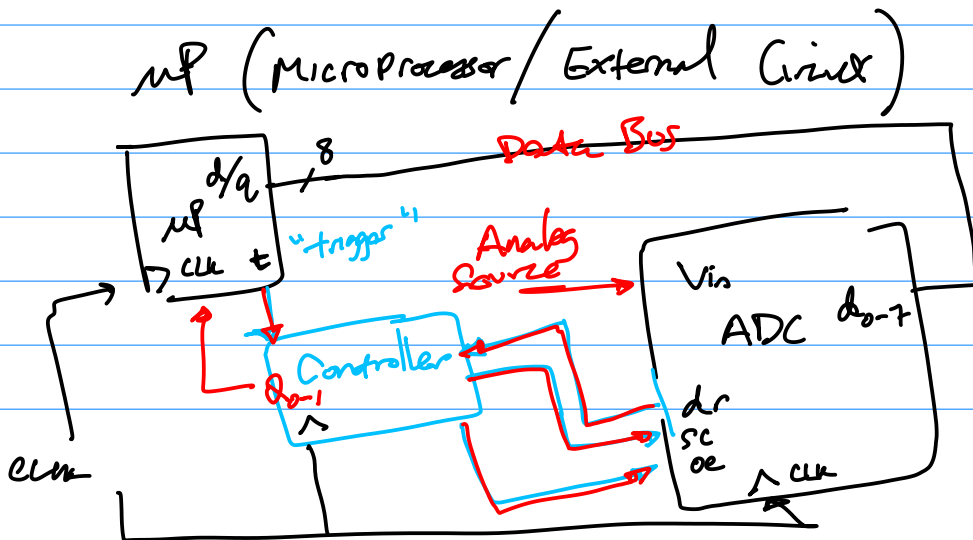
time to convert

- dr — Data Ready
- sc — Start Converting
- oe — Output Enable



MP (Microprocessor/External Circuit)

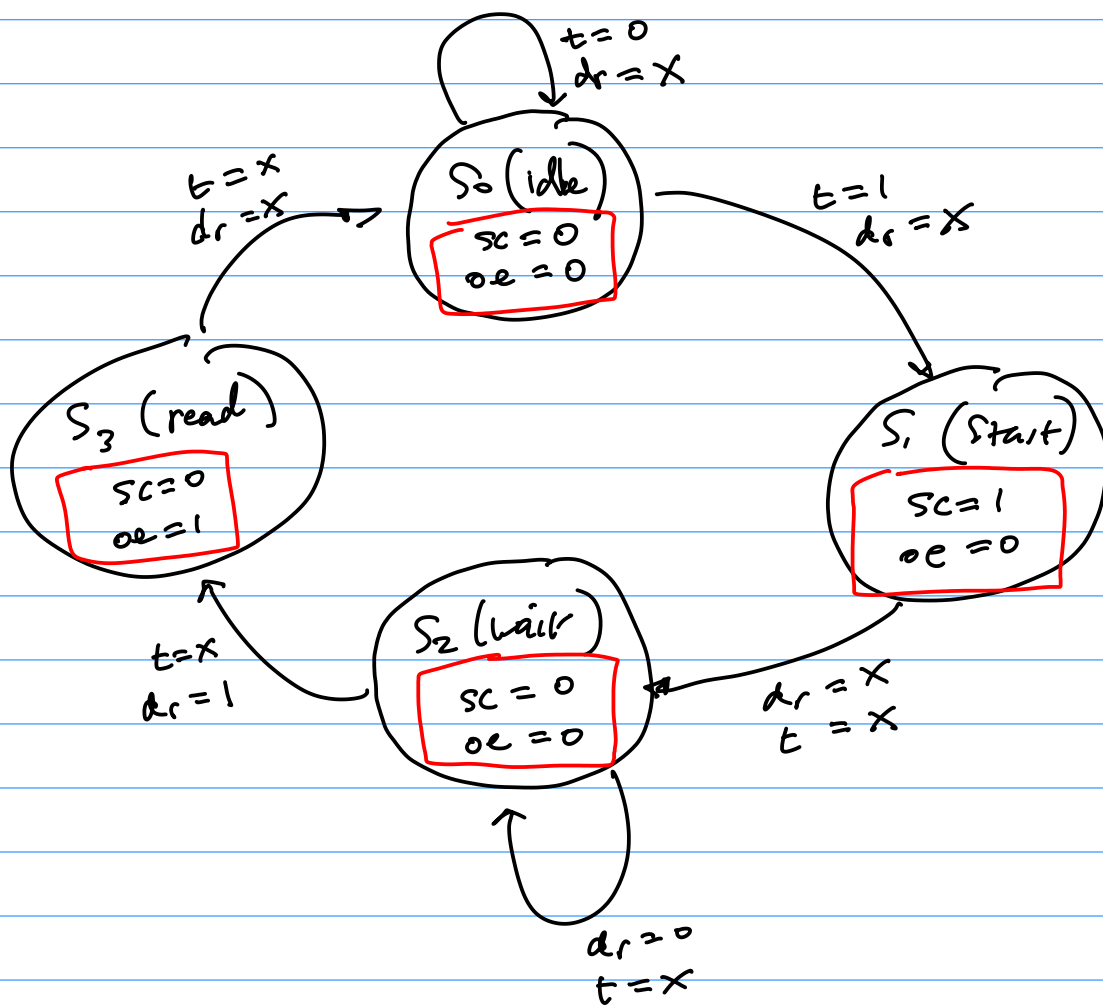
Other Circuits
Connected to Data bus



FB!

- 1) Tell the ADC to convert (upon trigger)
- 2) Wait until Data is ready
- 3) Enable ADC output
- 4) Read Data

State Transition Diagram:



bn

State	Input		State Var		Output		Control		State		
	t	dr	Q ₁	Q ₀	SC	OE	D ₁	D ₀	Q ₁	Q ₀	
S ₀	0	X	0	0	0	0	0	0	0	0	S ₀
S ₀	1	X	0	0	0	0	0	1	0	1	S ₁
S ₁	X	X	0	1	1	0	1	0	1	0	S ₂
S ₂	X	0	1	0	0	0	1	0	1	0	S ₂

S_2	X 1	1 0	∞	1 1	1 1	S_3
S_3	X X	1 1	0 1	0 0	0 0	S_0

$$[SC = \bar{Q}_1 \bar{Q}_0] \quad (\text{Start state})$$

$$[oe = Q_1 Q_0] \quad (\text{read state})$$

$$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{d}_r Q_1 \bar{Q}_0 + d_r Q_1 \bar{Q}_0$$

$$= \bar{Q}_1 \bar{Q}_0 + Q_1 \bar{Q}_0 (\bar{d}_r + d_r)$$

$$[D_1 = Q_1 \oplus Q_0] \quad \underbrace{\qquad\qquad\qquad}_1$$

$$[D_0 = \bar{Q}_1 \bar{Q}_0 + d_r Q_1 \bar{Q}_0]$$

