ECE 150 Digital Logic Design, Fall 2023

Midterm Exam, October 11th 2023 Name: _____

The exam has 100 pts. Closed book, no calculators. Write all answers and show all work inside your blue book. Read carefully.

Problem 1 (5 pts).
Convert the following to the specified number system.

(a) ADC_{16} to Octal.

(b) $0100\ 0101_2$ to Decimal.

(c) 909_{10} to Binary.

(d) 86_{10} to Hexadecimal.

(e) 132_4 to Decimal.

Problem 2 (5 pts).
Perform the following computation, $13_{10} - 25_{10}$, in a two's compliment binary number system. Verify that your answer is correct by converting your answer back to decimal.

Problem 3 (14 pts).
Consider the following boolean expression,

$$X = \overline{\overline{D} + B} + A(\overline{\overline{A} + BC}) + (D + \overline{B})\overline{C}B\overline{A}D$$

(a) Write X in a sum-of-products form.

(b) Convert X to a truth-table.

(c) Use a Karnaugh-map to simplify X from its truth table.

(d) Draw a logic diagram for the simplified expression. Label all inputs and outputs.

Problem 4 (8 pts).

(a) Write the truth-table, corresponding boolean expressions, and a logic symbol for a 1:2 **demux**.

(b) Draw the logic diagram of a 1:8 demux using your 1:2 demux symbols.

(c) Draw the logic diagram of a 1:16 demux using your 1:8 demuxes symbols.

Problem 5 (14 pts). For each of the follow gates, write an equivalent boolean expression using only NOR expressions, and draw the corresponding logic diagram (using only NOR gates).

(a) NOT

(b) OR

(c) AND

Problem 6 (20 pts).
In this problem, you will build a digital comparator that takes two N-bit binary numbers, A and B, and sets separate pins E, G, or L to high if $A = B$, $A > B$, or $A < B$, respectively.

(a) Write the truth-table for a *half-comparator* which takes as input two 1-bit binary numbers, A and B, and outputs E, G, and L.

(b) Determine boolean expressions of E and G. Express L in terms of E and G.

(c) A 1-bit *full-comparator* optionally takes as input the E and G results from another comparator (acting on more significant bits). Determine boolean expressions for the E, G, and L outputs of a 1-bit full-comparator in terms of A, B, E_{in}, and G_{in}.

(d) Draw a logic diagram for the 1-bit full-comparator. Draw a corresponding symbol to represent it.

(e) Draw a logic diagram for a 4-bit full-comparator, comparing $A_3A_2A_1A_0$ to $B_3B_2B_1B_0$ (left MSB), using 1-bit full comparators. Label all inputs and outputs. Do not leave input pins floating.

Problem 7 (4 pts).
Describe similarities and differences between the *SR-latch* and the *Gated D-Latch*.

Problem 8 (10 pts).
Consider the circuit shown in Figure 1, with a D-latch and Master-minion D Flip-Flop. Complete the timing for outputs Q_L and Q_F.

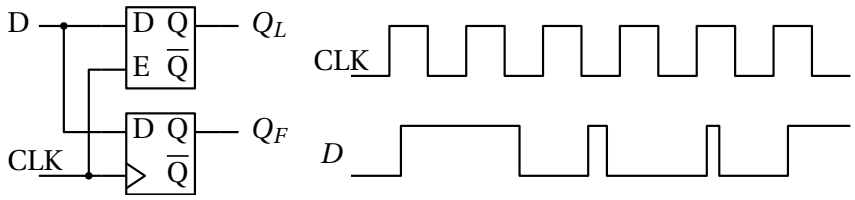

Figure 1: D-latch and MM D-FF circuit with corresponding input timing diagram.

Problem 9 (20 pts).
In this problem, you will build a synchronous "triggerable" Mod-4 binary **down** counter with positive edge-triggered D flip-flops. Specifically, from the $Q_1Q_0 = 11$ state the counter will only proceed to the next state when an external input T is high, otherwise it will remain in the 11 state. At all other states the input T has no effect on counting.

(a) Construct a state transition diagram for your counter.

(b) Convert your state transition digram to a table, labeling current states, inputs, control variables, and next states. Determine values for your control variables to achieve the desired transitions.

(c) Determine simplified boolean expressions for your control variables.

(d) Draw a logic diagram of your circuit. Label the clock, T, and your state variables clearly.