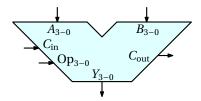
# ECE 150 Digital Logic Design, Fall 2023 **Project 1**: 4-bit Arithmetic Logic Unit Due October 4th 2023

Using any of the following ICs in JLab, gates, muxes, demuxes, decoders, implement a 4-bit Arithmetic Logic Unit (ALU) as a combinatorial logic circuit (no memory circuitry or sequential logic). Your ALU must accept two 4-bit words as input (A, B), a 4-bit op-code (Op) and output a single 4-bit word (Y).



Your ALU must be able to perform the following operations:

$$(Op=0000)$$
 No-op  $(Y=A)$   
 $(Op=0001)$  Binary Addition  $(Y=A+B)$   
 $(Op=0010)$  Binary Subtraction  $(Y=B-A,$  in two's complement)  
 $(Op=0011)$  Logical Shift of A (ex. if  $A=0101$ , then  $Y=101C_{\rm in}$ )  
 $(Op=0100)$  Bitwise OR  $(Y=A+B)$   
 $(Op=0101)$  Bitwise AND  $(Y=AB)$   
 $(Op=0110)$  Bitwise NOT  $(Y=\bar{A})$   
 $(Op=0111)$  Bitwise XOR  $(Y=A\oplus B)$ 

You will demonstrate the correct output of your circuit at the beginning of class on the due-date, and submit a typed PDF report.

### Circuit Requirements:

- Provide inputs  $A_{3-0}$ ,  $B_{3-0}$ , and  $Op_{3-0}$  via three 4-input DIP switches (active-high) from left to right.
- Use no more than four breadboards.
- Use red wire for 5V and black for ground.
- Display your outputs on LEDs.

## Report Requirements:

- Introduction: restate the problem in your own words
- Methods: detail how you arrived at your implementation. You must include,
  - truth-table(s)
  - a derivation of your final implemented expressions (boolean algebra or K-map)
  - logic diagram(s)
- Implementation: detail your circuit, including,
  - a picture of your circuit with labeled ICs and labeled subcircuits.
- Conclusion:
  - What are the pros and cons of your design?

# Grading:

- Correct circuit operation (demo) (40 pts)
- Report (60 pts)

## **Additional Considerations:**

#### • Circuit

- Can you combine ALUs with a classmate to create an 8-bit ALU? (+5 pts to project)
- (+3 pts to project) (Op = 1000) Arithmetic Shift of A (in two's complement) \* ex. if  $A = -3_{10}$ , then  $Y = -6_{10}$
- Neatness (color coding, right-angles only, no crossing wires) (+2/100 pts to midterm exam)
- Number of ICs used (+5/+3/+1) points to midterm for fewest chips used, ranked by class).

## • Report

- Consistent typesetting
- Schematics and diagrams done in CAD (or hand-drawn EXTREMELY NEATLY)
- Correct use of technical terms
- All Figures, Images, and Tables have captions and are referenced in the text

You may find it helpful to make use of simulation software, such as Logisim or Logisim-Evolution.