ECE 150 Digital Logic Design, Fall 2023
Project 2: Read/Write Cycle Finite-State-Machine
Due November 8th 2023

Using any of the CMOS or TTL integrated circuits (ICs) in JLab, including, *gates, flip-flops, counters, registers, muxes/demuxes, 555 timers*, implement a sequential logic circuit that,

(1) Writes a byte into a 4 bit-per-word (bpw) RAM chip upon a single press from a *write-button*.
(2) Reads a byte from a 4 bpw RAM chip into external parallel-out registers, upon a single press from a *read-button*.

Circuits will be demonstrated at the start of class on the due date. The report will be due at midnight. A penalty of -1 pts will be applied for every day the report is late.

Circuit Requirements:

- Use a **single 2114 SRAM** IC.
- Provide data inputs via DIP switches.
- Use no more than four breadboards.
- Use red wire for 5V and black for ground.
- Continuously display the contents of your external parallel-out registers on LEDs.
- All buttons must be debounced.
- TTL to CMOS interfaces properly accounted for (i.e. level conversion if required. See *74LS07 Hex buffer w/ open collector.*).

Report Requirements:

- Adhere to the following outline:
  1 **Introduction**: restate the problem in your own words. Briefly introduce your approach and give an outline of the following sections.
  2 **Methods**: detail how you arrived at your implementation. You must include,
    - Theory: Why do we employ finite-state-machines for interfacing with RAM? Why do we use external registers as the output interface?
    - State-diagram(s) and state transition table(s)
    - Truth-tables, boolean expressions, and logic diagrams.
    - Functional block diagram(s)
  3 **Implementation**: detail your circuit, including,
    - a picture of your circuit with components labeled.
    - explanation of TTL-CMOS interfacing if used.
  4 **Conclusion**:
    - Summarize the problem and your implemented solution. Discuss the limitations of your design. Suggest how this work may be used in a larger system/circuit.

Grading:

- Valid state-diagram(s) + state-transition table(s) (20 pts)
- In-class demo of circuit (40 pts), 20 pts guaranteed if Logisim simulation demonstrated in-person (before class or office-hours) at least 1 week before the due date.
- Report (40 pts)

Additional Considerations:

- Circuit
  - Neatness (color coding, right-angles only, no crossing wires)
  - Design choice(s) which improve user experience (audio/visual feedback) and/or provide additional circuit functionality.
- Report
  - Consistent typesetting
  - Schematics and diagrams done in CAD (or hand-drawn EXTREMELY NEATLY)
  - Correct use of technical terms
  - All tables and figures referenced in the text and accompanied by a caption.
  - Technical writing voice.