## ECE 150 Digital Logic Design, Fall 2023 Quiz 2, October 4th 2023

## **Problem 1** (10 pts).

Consider the Mod-N counter in Fig. 1 below.

- (a) (2 pts) Is this circuit synchronous or asynchronous?
- (b) (6 pts) With FF outputs labeled  $Q_2Q_1Q_0$  left to right, draw a timing diagram to determine the states of the counter, assuming  $Q_2Q_1Q_0 = 111$  at initialization.
- (c) (1 pts) Denote the FF states below your timing diagram in decimal, interpreting  $Q_2$  as the MSB and  $Q_0$  as the LSB.
- (d) (1 pts) What Mod is the counter?

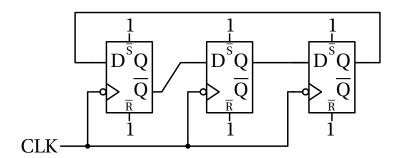


Figure 1: Counter circuit with start-up reset configuration.