ECE 150 Digital Logic Design, Fall 2024

Midterm Exam, October 16th 2024 Name: _____

The exam has 90 pts. Closed book, no calculators. Write all answers and show all work inside your blue book. Read carefully.

Problem 1 (6 pts).
Convert the following to the specified number system.

(a) $1001\ 0111_2$ to Decimal.

(b) 321_{10} to Binary.

(c) 73_{10} to Hexadecimal.

Problem 2 (6 pts).
Perform the following computation, $15_{10} - 25_{10}$, in a two's compliment binary number system. Verify that your answer is correct by converting your answer back to decimal.

Problem 3 (14 pts).
Consider the following boolean expression,

$$X = \overline{\overline{C} + B} + A(\overline{\overline{A} + DC}) + (A + \overline{B})\overline{A}B\overline{C}D$$

(a) Write X in a sum-of-products form.

(b) Convert X to a truth-table.

(c) Use a Karnaugh-map to simplify X from its truth table.

(d) Draw a logic diagram for the simplified expression. Label all inputs and outputs.

Problem 4 (10 pts).

(a) Write the truth-table, boolean expression, and a logic symbol for a 2:1 **mux**.

(b) Draw the logic diagram of a 8:1 mux using your 2:1 mux symbols.

Problem 5 (14 pts). For each of the follow gates, write an equivalent boolean expression using only NAND expressions, and draw the corresponding logic diagram (using only NAND gates).

(a) NOT

(b) OR

Problem 6 (20 pts).
In this problem, you will build a digital comparator that takes two N-bit binary numbers, A and B, and sets separate pins E, G, or L to high if $A = B$, $A > B$, or $A < B$, respectively.

(a) Write the truth-table for a *half-comparator* which takes as input two 1-bit binary numbers, A and B, and outputs E, G, and L.

(b) Determine boolean expressions of E and G. Express L in terms of E and G.

(c) A 1-bit *full-comparator* optionally takes as input the E and G results from another comparator (acting on more significant bits). Determine boolean expressions for the E, G, and L outputs of a 1-bit full-comparator in terms of A, B, E_{in}, and G_{in}.

(d) Draw a logic diagram for the 1-bit full-comparator. Draw a corresponding symbol to represent it.

(e) Draw a logic diagram for a 4-bit full-comparator, comparing $A_3A_2A_1A_0$ to $B_3B_2B_1B_0$ (left MSB), using 1-bit full comparators. Label all inputs and outputs. Do not leave input pins floating.

Problem 7 (10 pts).
Consider the circuit shown in Figure 1, with a D-latch and Master-minion D Flip-Flop. Complete the timing for outputs Q_L and Q_F.

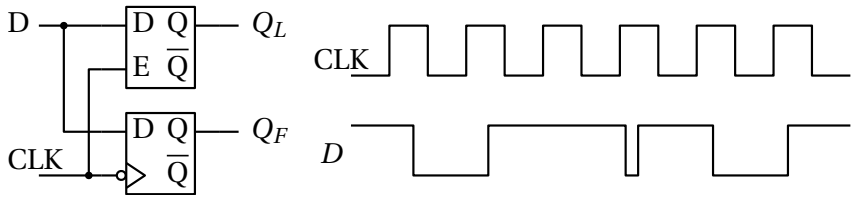

Figure 1: D-latch and MM D-FF circuit with corresponding input timing diagram.

Problem 8 (10 pts).
In the following questions, provide truth tables in terms of current state Q_n, control variables (D or J and K), and next state Q_{n+1}.

(a) Give the truth table of a negative edge-triggered D flip-flop.

(b) Give the truth table of a negative edge-triggered JK flip-flop.

(c) Using a single positive edge-triggered D flip-flop (plus any gates and muxes/de-muxes), implement a positive edge-triggered JK flip-flop.

(d) Using additional gates, how can you augment the circuit from (c) to be positive edge-triggered?