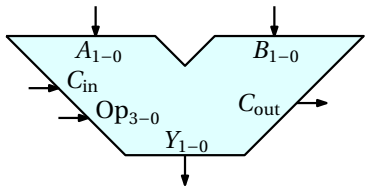
ECE 150 Digital Logic Design, Fall 2024
Project 1: 2-bit Arithmetic Logic Unit
Due October 9th 2024

Using any of the following ICs in JLab, *gates, muxes, demuxes, decoders*, implement a 2-bit Arithmetic Logic Unit (ALU) as a combinatorial logic circuit (no memory circuitry or sequential logic). Your ALU must accept two 2-bit words as input (A, B), a 4-bit op-code (Op) and output a single 2-bit word (Y).



Your ALU must be able to perform the following operations:

($Op = 0000$) No-op ($Y = A$)
($Op = 0001$) Binary Addition ($Y = A + B$)
($Op = 0010$) Binary Subtraction ($Y = B - A$, in two's complement)
($Op = 0011$) Logical Shift of A (ex. if $A = 01$, then $Y = 1C_{\text{in}}$)
($Op = 0100$) Bitwise OR ($Y_n = A_n + B_n$)
($Op = 0101$) Bitwise AND ($Y_n = A_n B_n$)
($Op = 0110$) Bitwise NOT ($Y_n = \bar{A}_n$)
($Op = 0111$) Bitwise XOR ($Y_n = A_n \oplus B_n$)

You will demonstrate the correct output of your circuit at the beginning of class on the due-date, and submit a typed PDF report.

Circuit Requirements:

- Provide inputs A_{1-0}, B_{1-0}, and Op_{3-0} via three 4-input DIP switches (active-high) from left to right.
- Use no more than three breadboards.
- Use red wire for 5V and black for ground.
- Display your outputs on LEDs.

Report Requirements:

- Introduction: restate the problem in your own words
- Methods: detail how you arrived at your implementation. You must include,
  - truth-table(s)
  - a derivation of your final implemented expressions (boolean algebra or K-map)
  - logic diagram(s)
- Implementation: detail your circuit, including,
  - a picture of your circuit with labeled ICs and labeled subcircuits.
- Conclusion:
  - What are the pros and cons of your design?

Grading:

- Correct circuit operation (demo) (45 pts)
- Report (45 pts)
- Scalable ALU (see additional circuit considerations below) (10 pts)

Additional Considerations:

- Circuit
  - **Scalable ALU**: Can you combine ALUs with a classmate to create an 4-bit ALU? An 8-bit ALU? (+5 pts to project if 4-bit ALU demo'd, +5pts to project if 2N-bit ALU described in report)
  - Neatness (color coding, right-angles only, no crossing wires) (+2/100 pts to midterm exam)
  - Number of ICs used (+3/+1 points to midterm for fewest chips used, ranked by class).
- Report
  - Consistent typesetting
  - Schematics and diagrams done in CAD (or hand-drawn EXTREMELY NEATLY)
  - Correct use of technical terms
  - All Figures, Images, and Tables have captions and are referenced in the text

You may find it helpful to make use of simulation software, such as Logisim or Logisim-Evolution.