ECE-150 Digital Logic Design, Fall 2025

Midterm Exam, October 16th 2025 Name: _____

The exam has 90 pts. Closed book, no calculators. Write all answers and show all work in your blue book. Read carefully.

Problem 1 (6 pts).

Convert the following to the specified number system.

(a) $1101\ 0110_2$ to Decimal.

(b) 375_{10} to Binary.

(c) $5E_{16}$ to Octal.

Problem 2 (6 pts).

Perform $23_{10} - 30_{10}$ using a 6-bit two's complement numbering system. Verify correctness by converting the result back to decimal.

Problem 3 (14 pts).

Simplify the following Boolean expression:

$$Y = (A + \overline{B})(C + D) + \overline{AC} + BD$$

(a) Write Y in canonical sum-of-products form.

(b) Construct the truth table.

(c) Simplify Y using a Karnaugh map.

(d) Draw the logic diagram for the simplified form.

Problem 4 (10 pts).

Muxes.

(a) Write the truth table and derive boolean expressions for a 2:1 multiplexer.

(b) Draw a logic diagram of your 2:1 mux and give it a symbol.

(c) Draw an 8:1 multiplexer using only 2:1 multiplexers and any necessary logic gates.

Problem 5 (12 pts).

Express each of the following gates using only NAND gates. Then draw the corresponding circuit:

(a) NOT

(b) OR

(c) XOR

Problem 6 (14 pts).
Design a circuit that outputs 1 if a 4-bit unsigned number is a multiple of 3.

(a) Write the truth table.

(b) Derive a simplified Boolean expression using a K-map.

(c) Draw the resulting logic diagram.

Problem 7 (14 pts).
A 3-bit ripple counter is constructed using positive-edge triggered D flip-flops (D-FFs). Label the output of the first D-FF (clocked by CLK) as Q_0. Each subsequent D-FF is clocked by the previous' Q.

(a) Draw the circuit diagram.

(b) Derive the count sequence with a timing diagram starting in the Q=000 state. Indicate any glitch states.

(c) Label each state with a corresponding decimal value.

Problem 8 (14 pts).
A bidirectional shift register is a synchronous circuit in which data can be clocked into D Flip-Flops if a parallel load signal P=1. Otherwise, input S dictates if a clock signal shifts data forward or backward (B=1 backward), (B=0 forward). With D-FFs, gates, and muxes/demuxs at your disposal,

(a) Design a 3-bit bidirectional shift register. Carefully label your parallel inputs ($A_2A_1A_0$), your serial inputs, and your control signals.

(b) Encapsulate your design in a symbol.

(c) Create a 6-bit bidirectional shift register using your 3-bit bidi registers.