ECE-150 Digital Logic Design, Fall 2025
Project 1: 2-bit Arithmetic Logic Unit
Due October 9th 2025

Using any of the following ICs in JLab, *gates, muxes, demuxes, decoders*, implement a 2-bit Arithmetic Logic Unit (ALU) as a combinatorial logic circuit (no memory circuitry or sequential logic). Your ALU must accept two 2-bit words as input (A, B), a 4-bit op-code (Op) and output a single 2-bit word (Y), as shown in Figure 1 below.

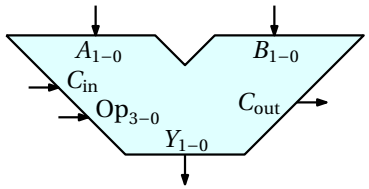

Figure 1: Block diagram of 2-Bit ALU with inputs and outputs.

Your ALU must be able to perform the following operations:

($Op = 0000$) No-op ($Y = A$)
($Op = 0001$) Binary Addition ($Y = A + B$)
($Op = 0010$) Binary Subtraction ($Y = B - A$, in two's complement)
($Op = 0011$) Logical Shift of A (ex. if $A = 01$, then $Y = 1C_{\text{in}}$)
($Op = 0100$) Bitwise OR ($Y_n = A_n + B_n$)
($Op = 0101$) Bitwise AND ($Y_n = A_n B_n$)
($Op = 0110$) Bitwise NOT ($Y_n = \bar{A}_n$)
($Op = 0111$) Bitwise XOR ($Y_n = A_n \oplus B_n$)

You will demonstrate the correct output of your circuit at the beginning of class and submit a typed PDF report on the due-date.

Grading:

- Correct circuit operation (demo) (45 pts)
- Report (45 pts)
- Scalable ALU (see Additional Considerations below) (10 pts)

Circuit Requirements:

- Provide inputs A_{1-0}, B_{1-0}, and Op_{3-0} via three 4-input DIP switches (active-high) from left to right.
- Use no more than three breadboards.
- Use red wire for 5V and black for ground.
- Display your outputs on LEDs.

Report Requirements:

- *Introduction*:
  - Restate the project.
  - Include background information about your circuit.
  - Specify what your report includes.
- *Methods*: Detail your logic, including,
  - truth-table(s),
  - a derivation of your final implemented expressions (boolean algebra or K-map),
  - and logic diagram(s).
- *Implementation*: Detail your circuit, including,
  - a picture of your circuit with labeled ICs
  - and a picture of your circuit with labeled sub-circuits.
- *Discussion and Conclusion*:
  - What was implemented?
  - What engineering/design choices were made?
  - What are the implementation's strengths and weaknesses?

Additional Considerations:

- Circuit
  - *Scalable ALU*: Combine ALUs with a classmate to create a 4-bit ALU.
    - 4-bit ALU demonstrated (+5 pts to project)
    - 2N-bit ALU described in report (+5 pts to project)
  - *Neatness*:
    - color coding (+1/100 pts to midterm exam)
    - right-angles only (+1/100 pts to midterm exam)
    - no crossing wires (+1/100 pts to midterm exam)
  - *Number of ICs Used*: (ranked by class)
    - Least chips used (+3/100 pts to midterm exam)
    - Second least chips used (+1/100 pts to midterm exam)
- Report
  - Technical writing voice used
  - Consistent typesetting
  - Schematics and diagrams done in CAD
  - Correct use of technical terms demonstrating understanding of material
  - All Figures, Images, and Tables have captions and are referenced in the text
  - Abbreviations are introduced in full

You may find it helpful to make use of simulation software, such as Logisim or Logisim-Evolution.